2002-0202-2003-1

Fig. 1

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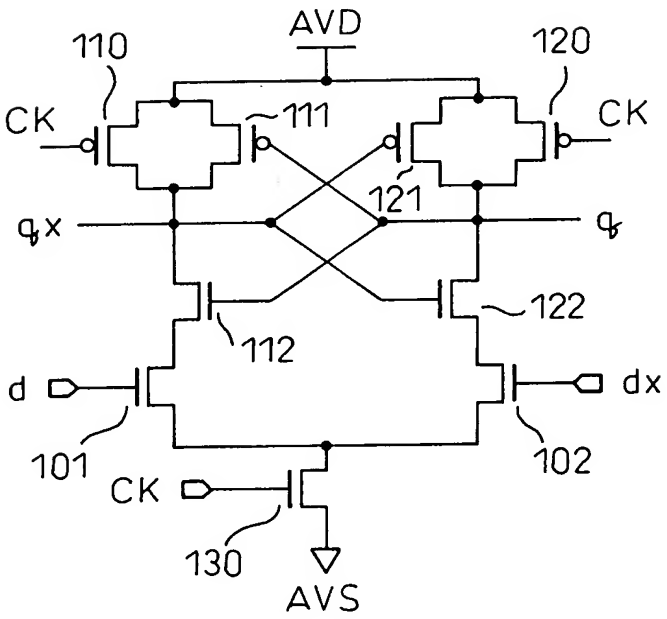

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Fig.2

(PRIOR ART)

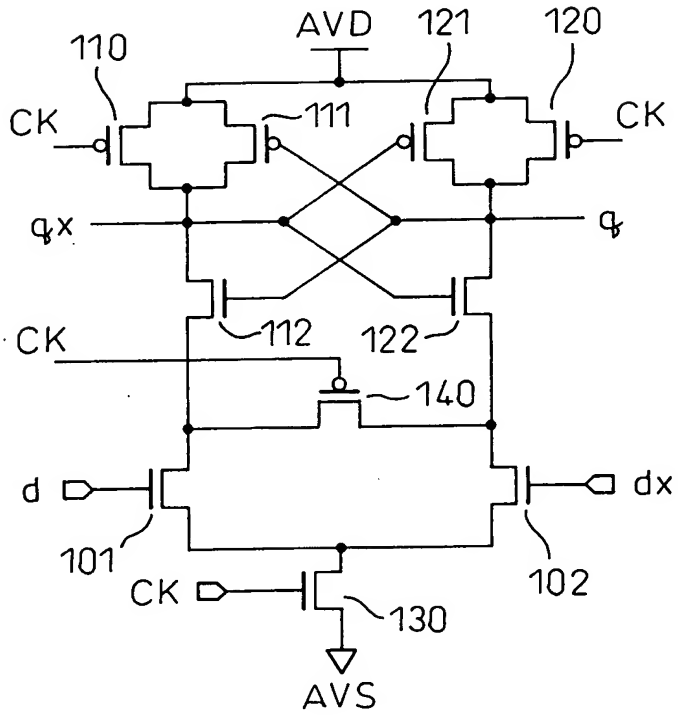

Fig.3
(PRIOR ART)

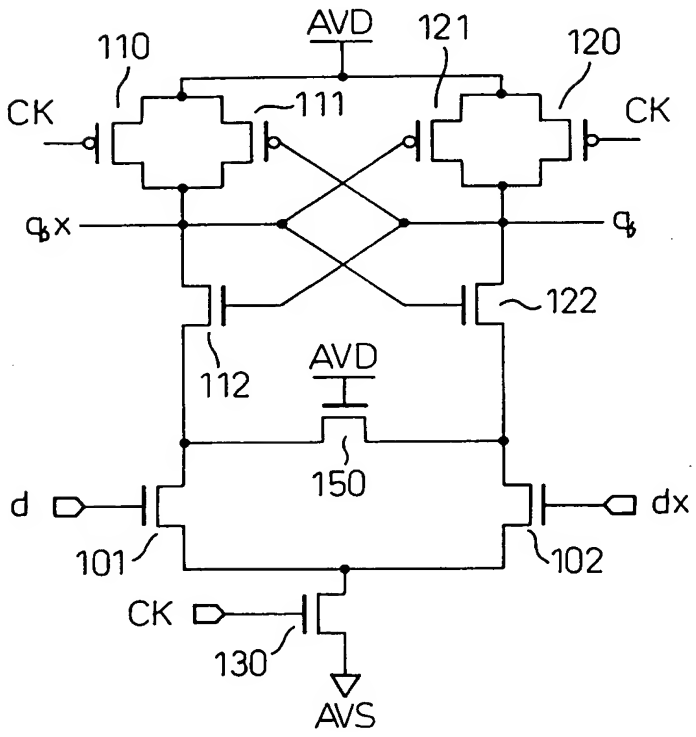

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Fig.4

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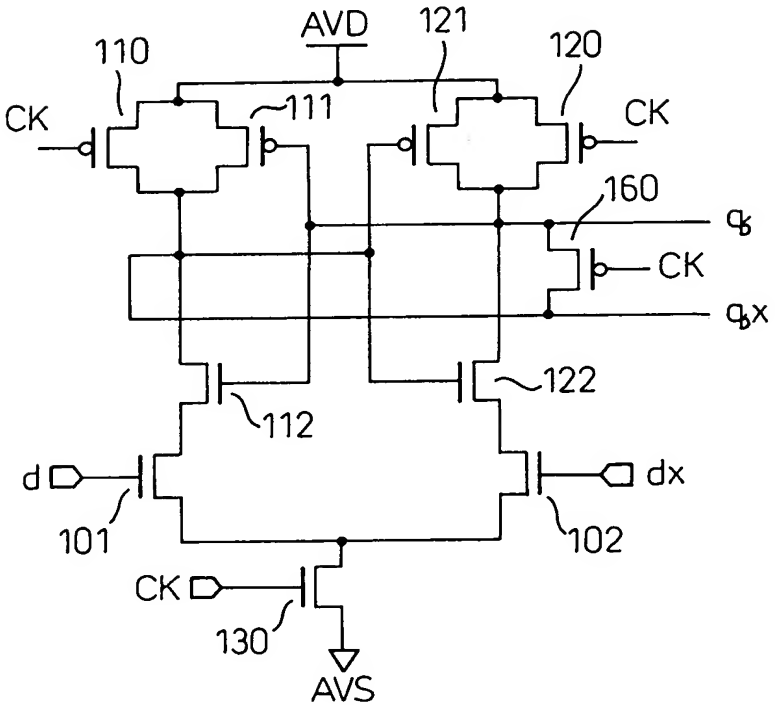

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Fig.5

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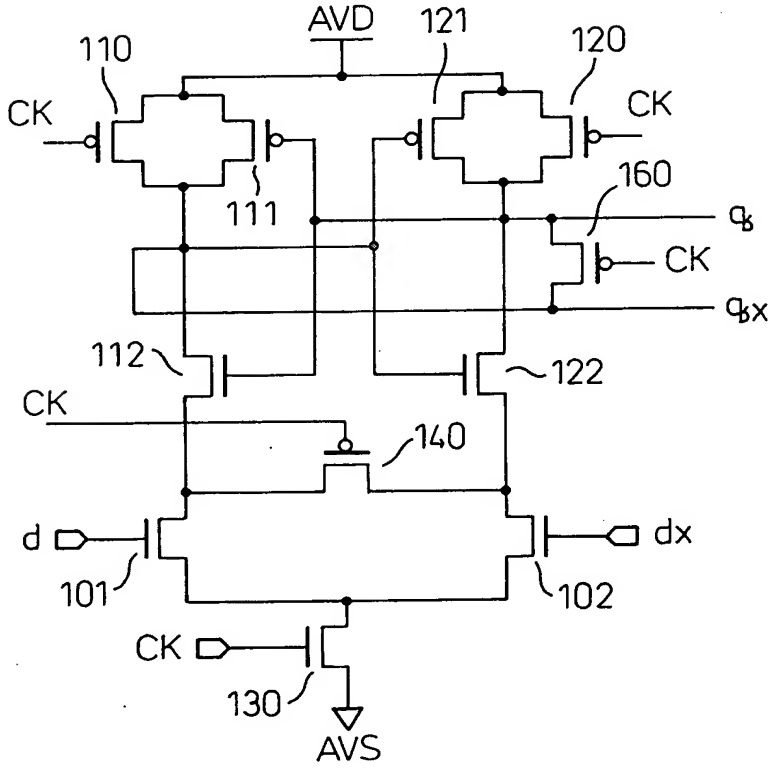

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Fig.6

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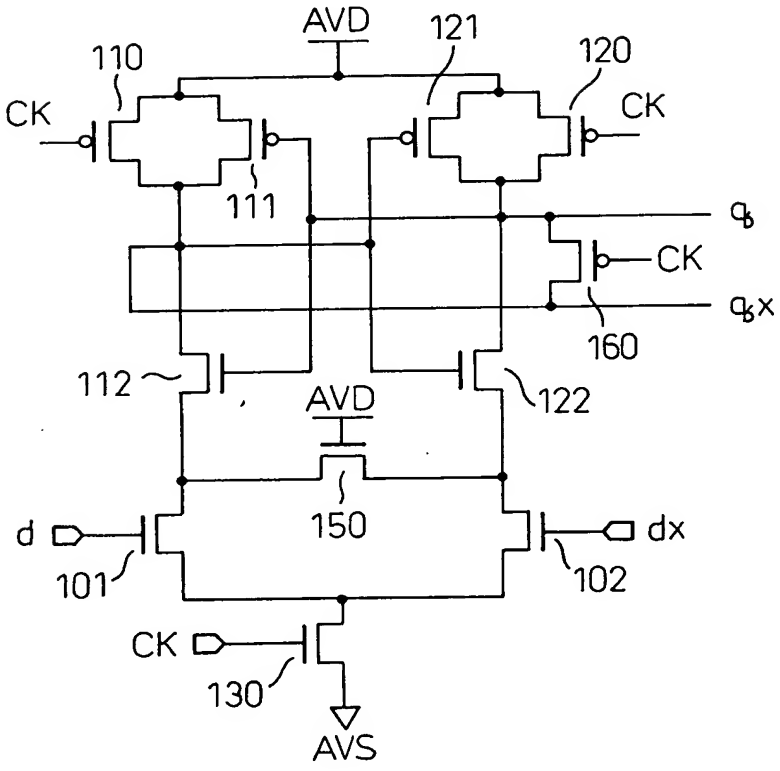

JP02-253620

Fig. 7

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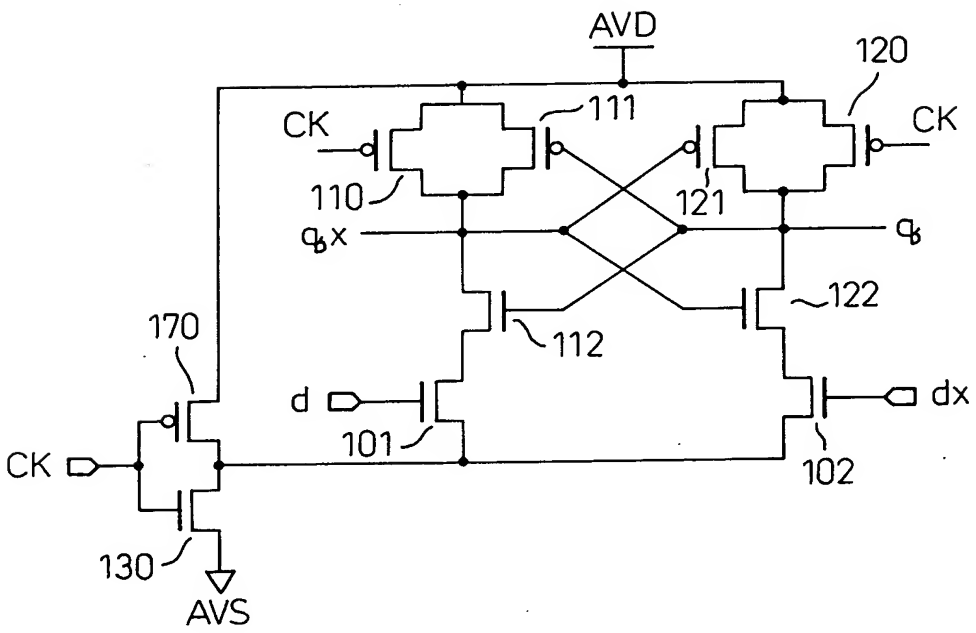


JP02212202 : 02.12.2002

Fig.8

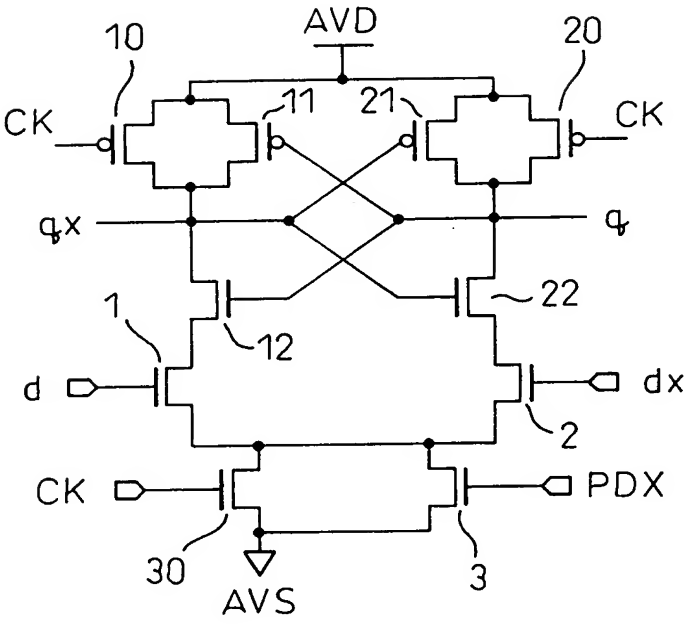


Fig.9

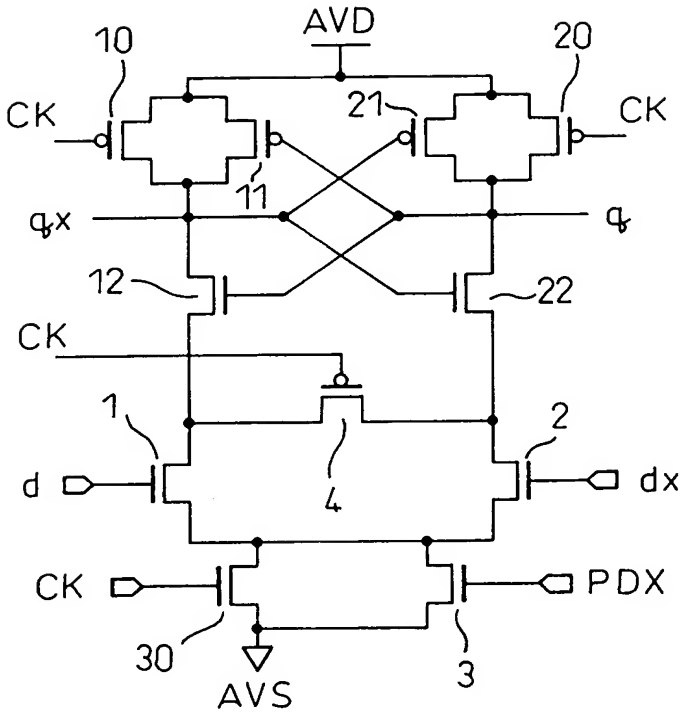


Fig.10

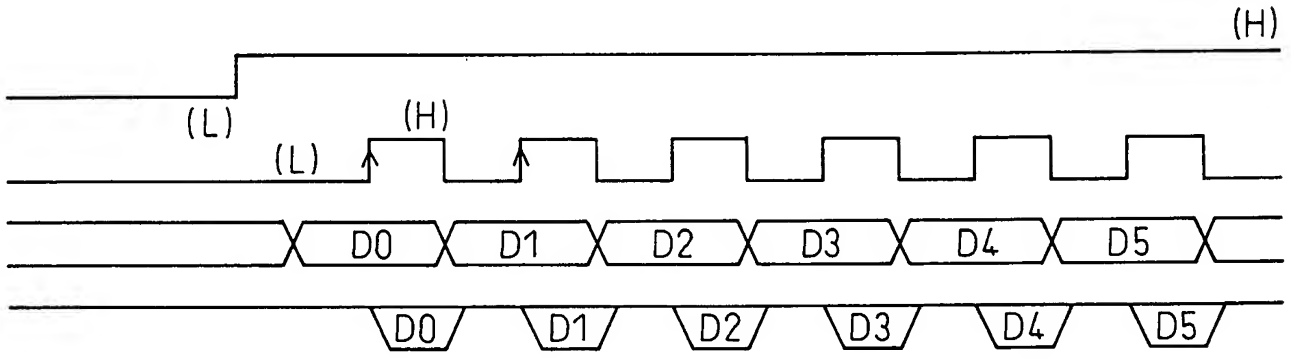
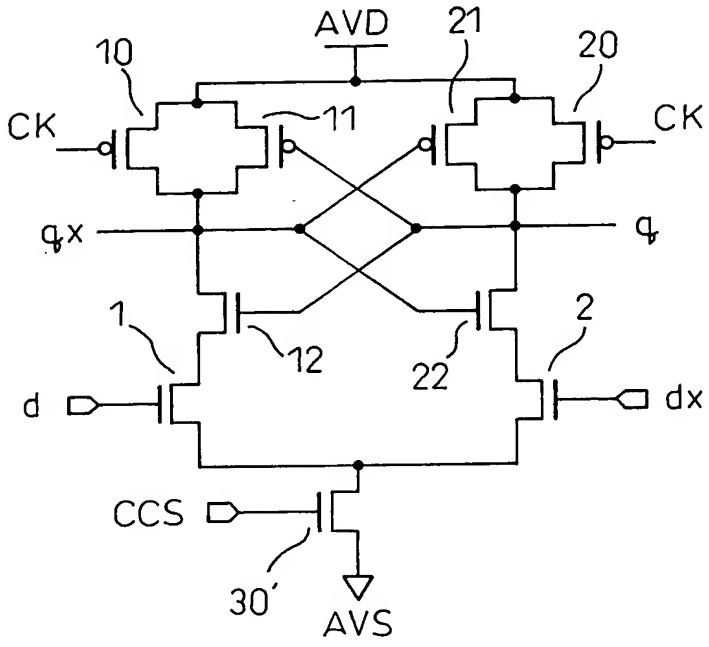


Fig.11A



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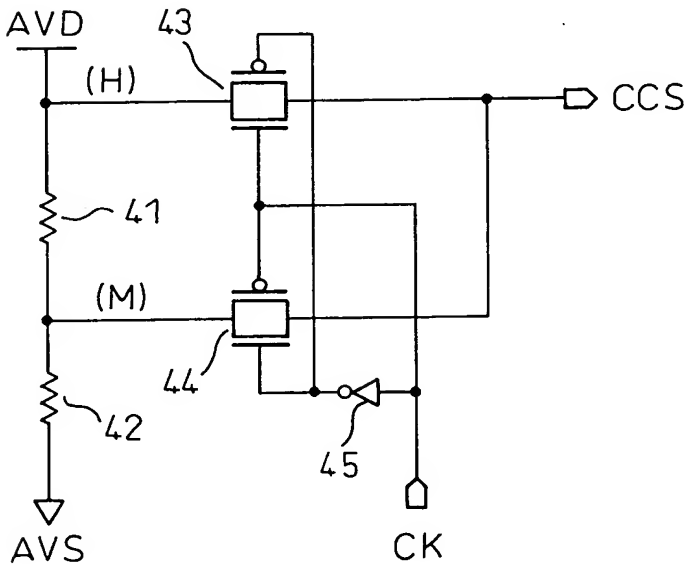

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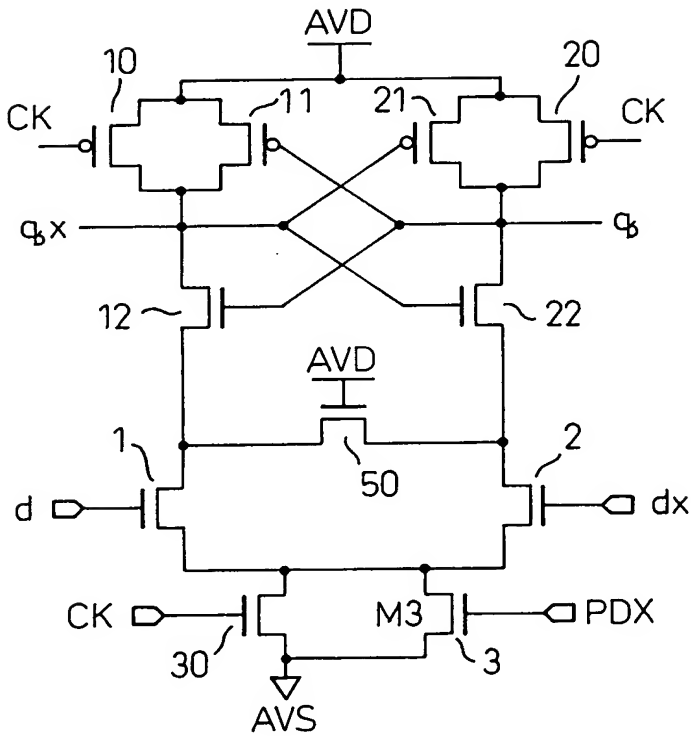
Fig.12

Fig.13



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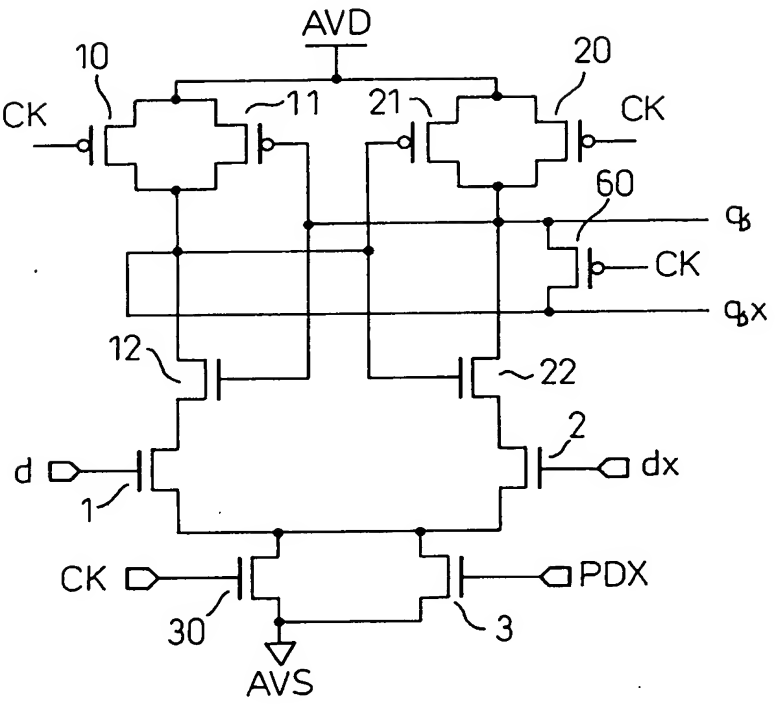

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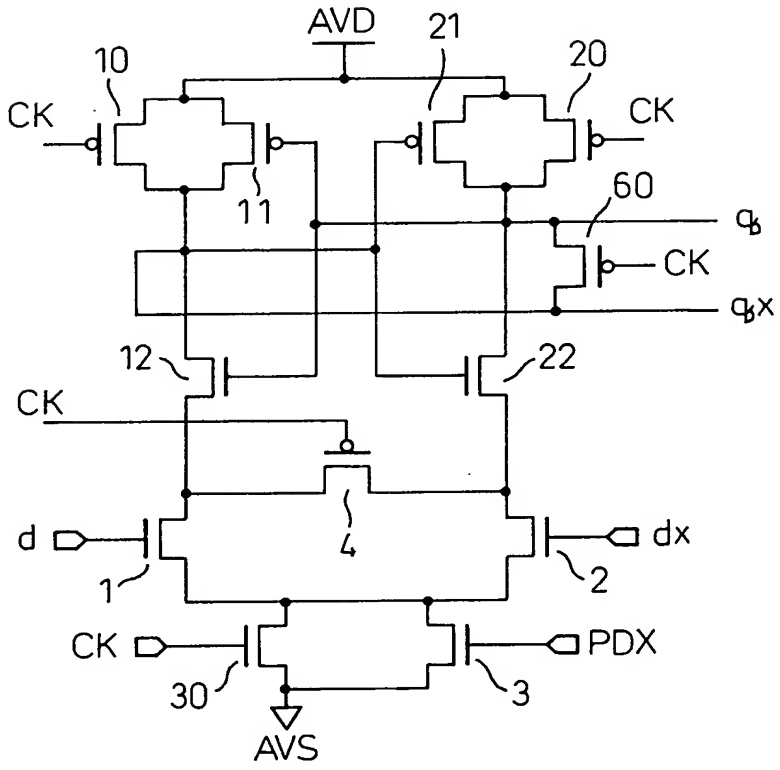

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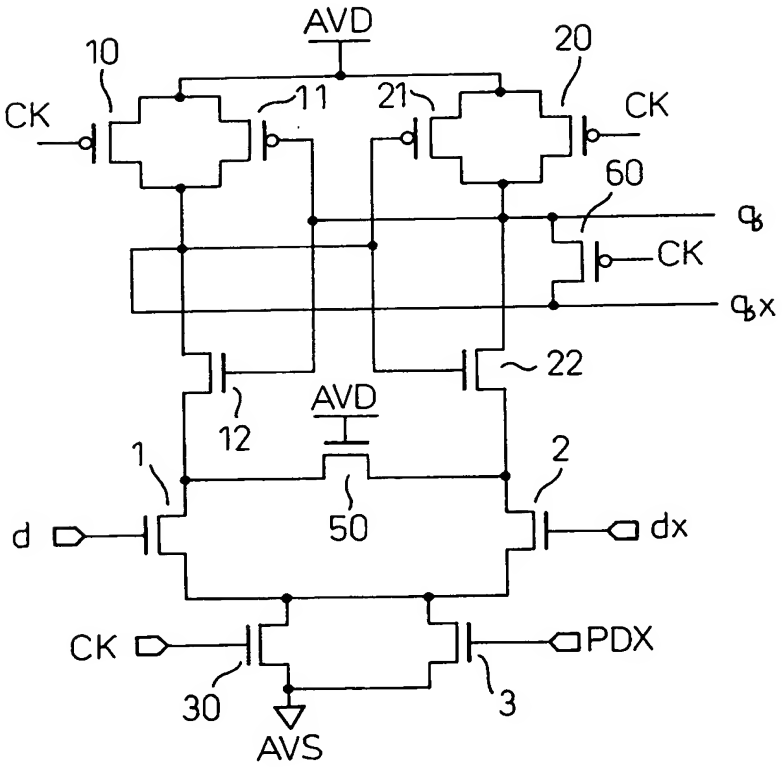
Fig.16



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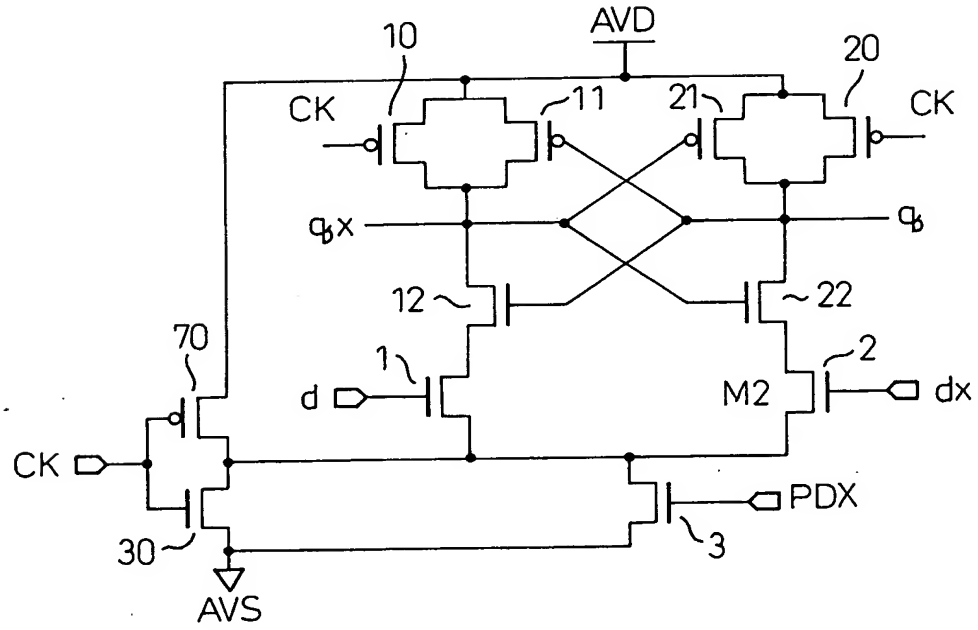

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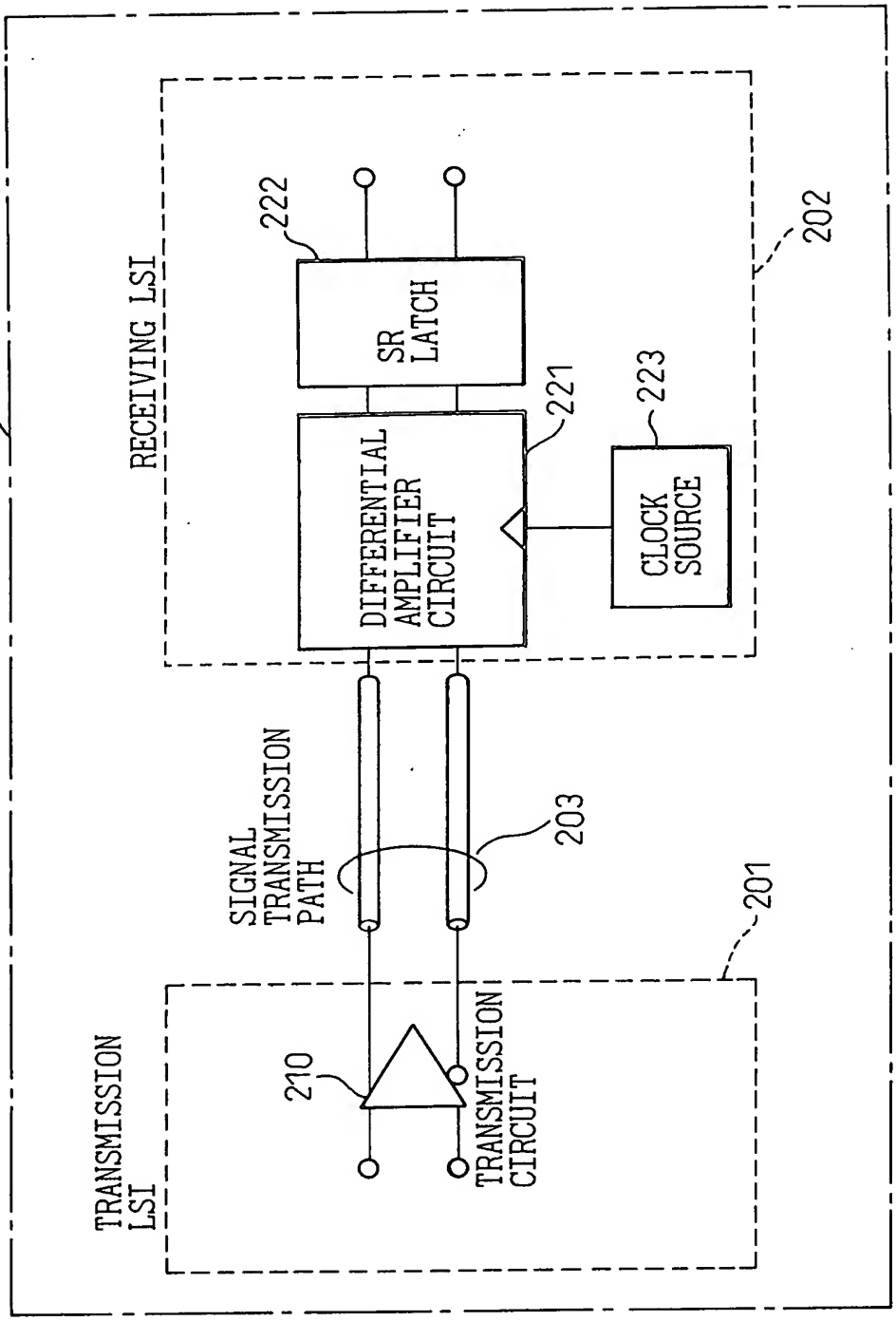
Fig. 18



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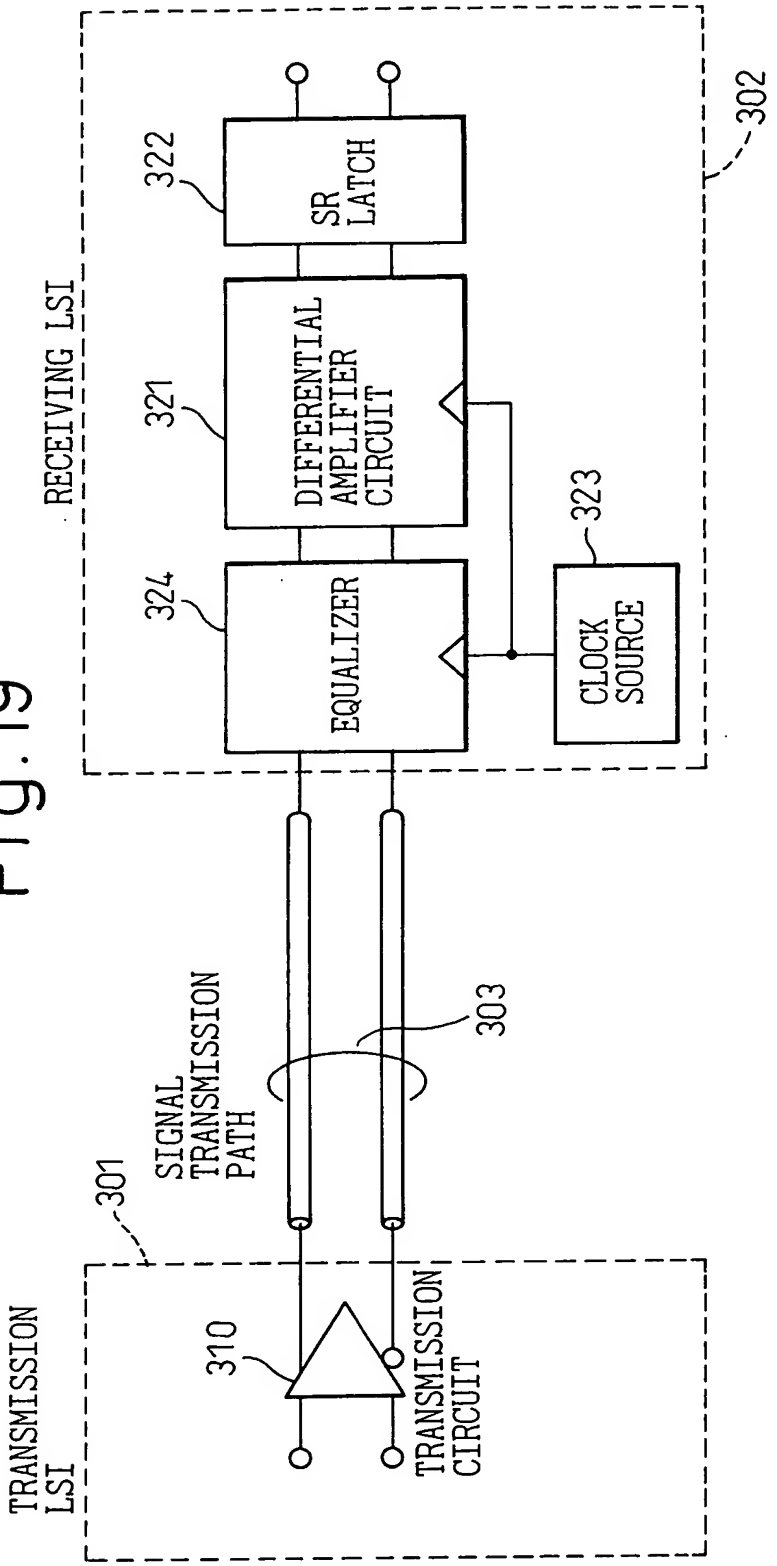

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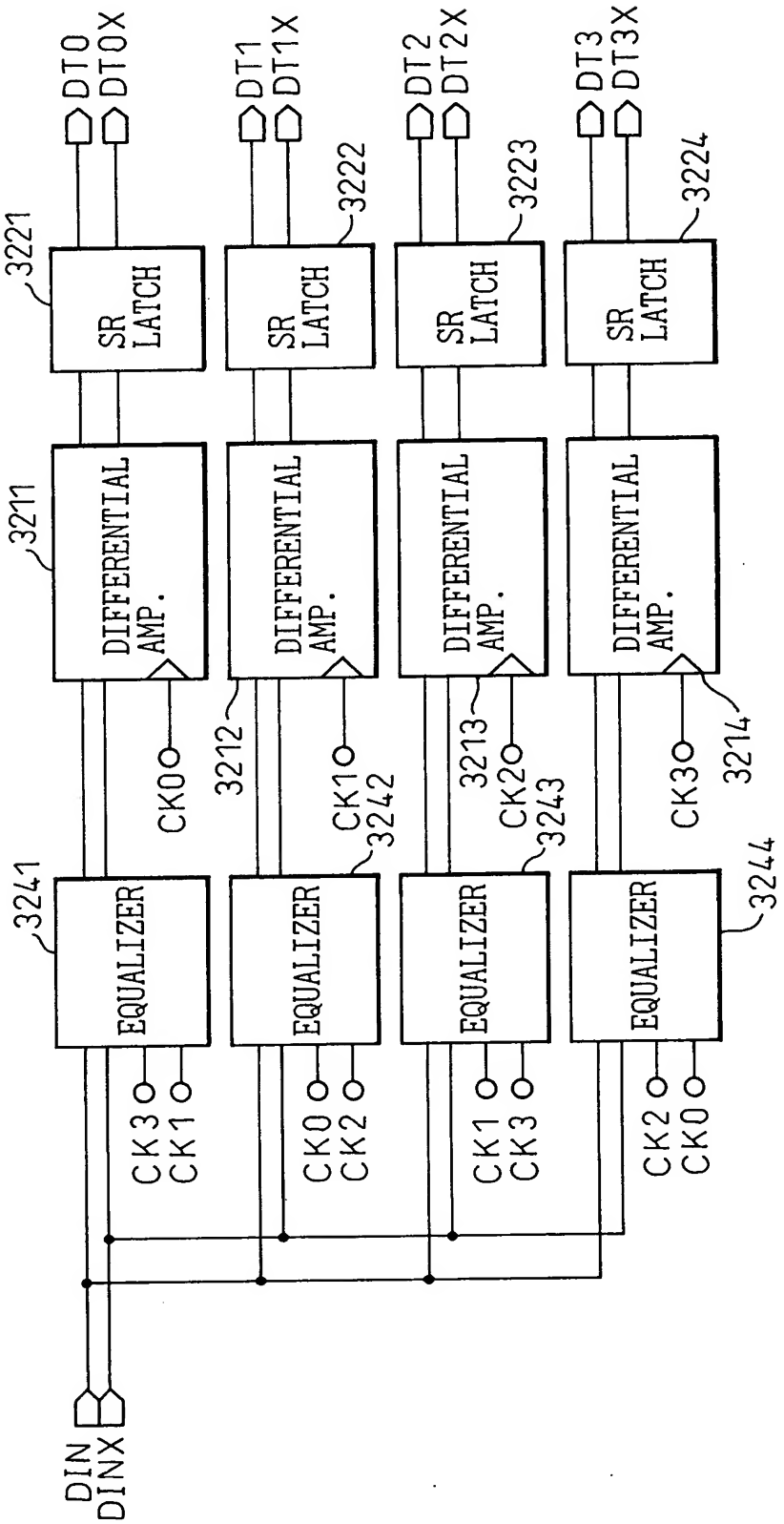
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CK3
SR LATCH
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DT0
DT0X
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Fig.21

3241

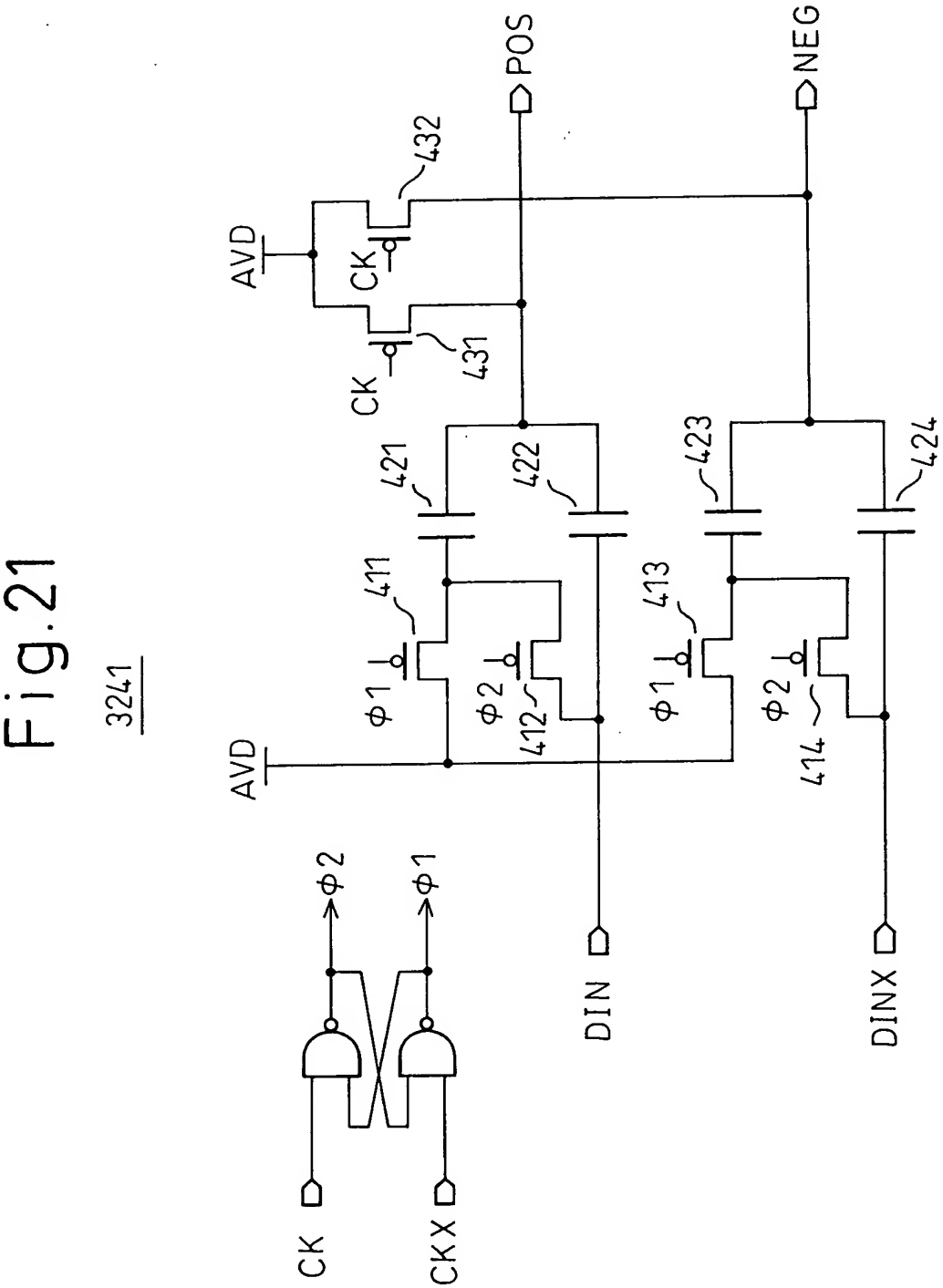

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Fig.22

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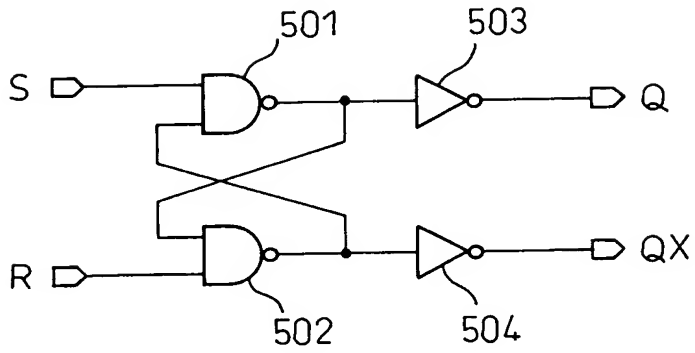

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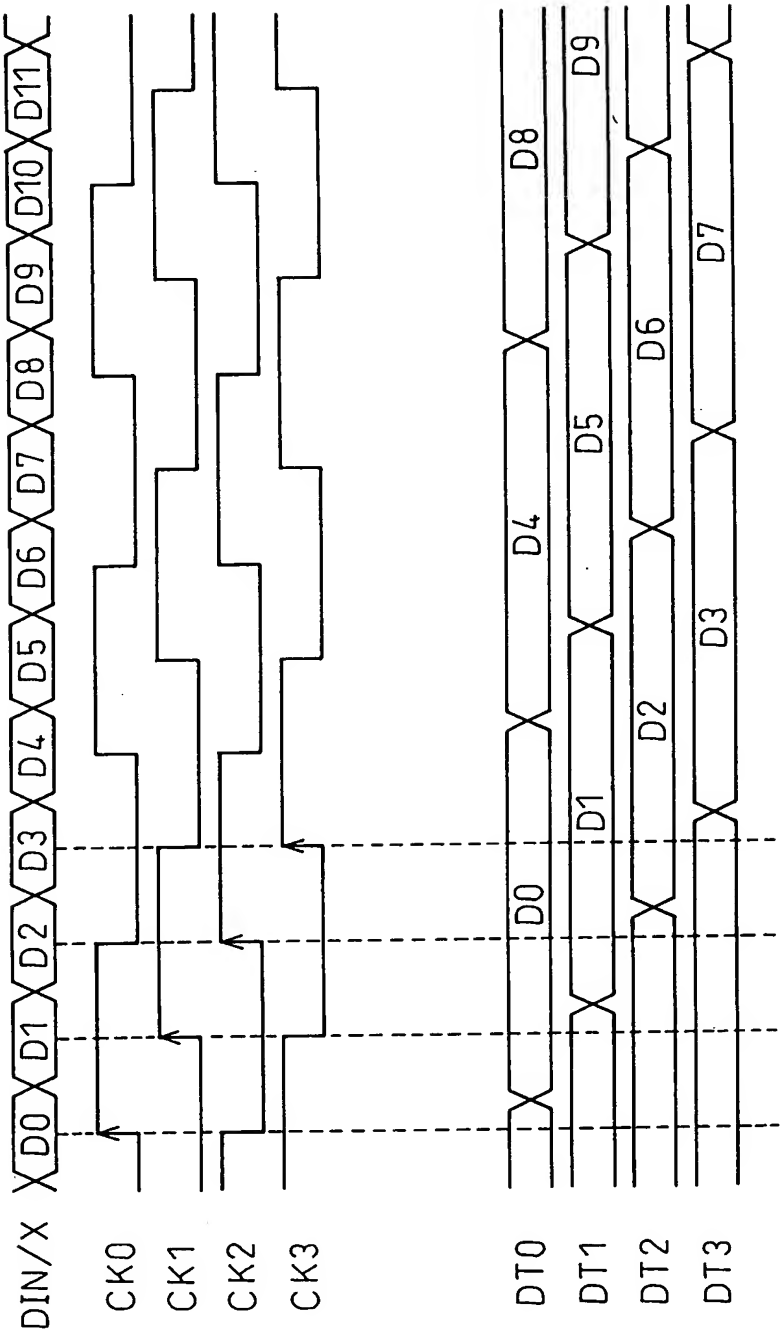

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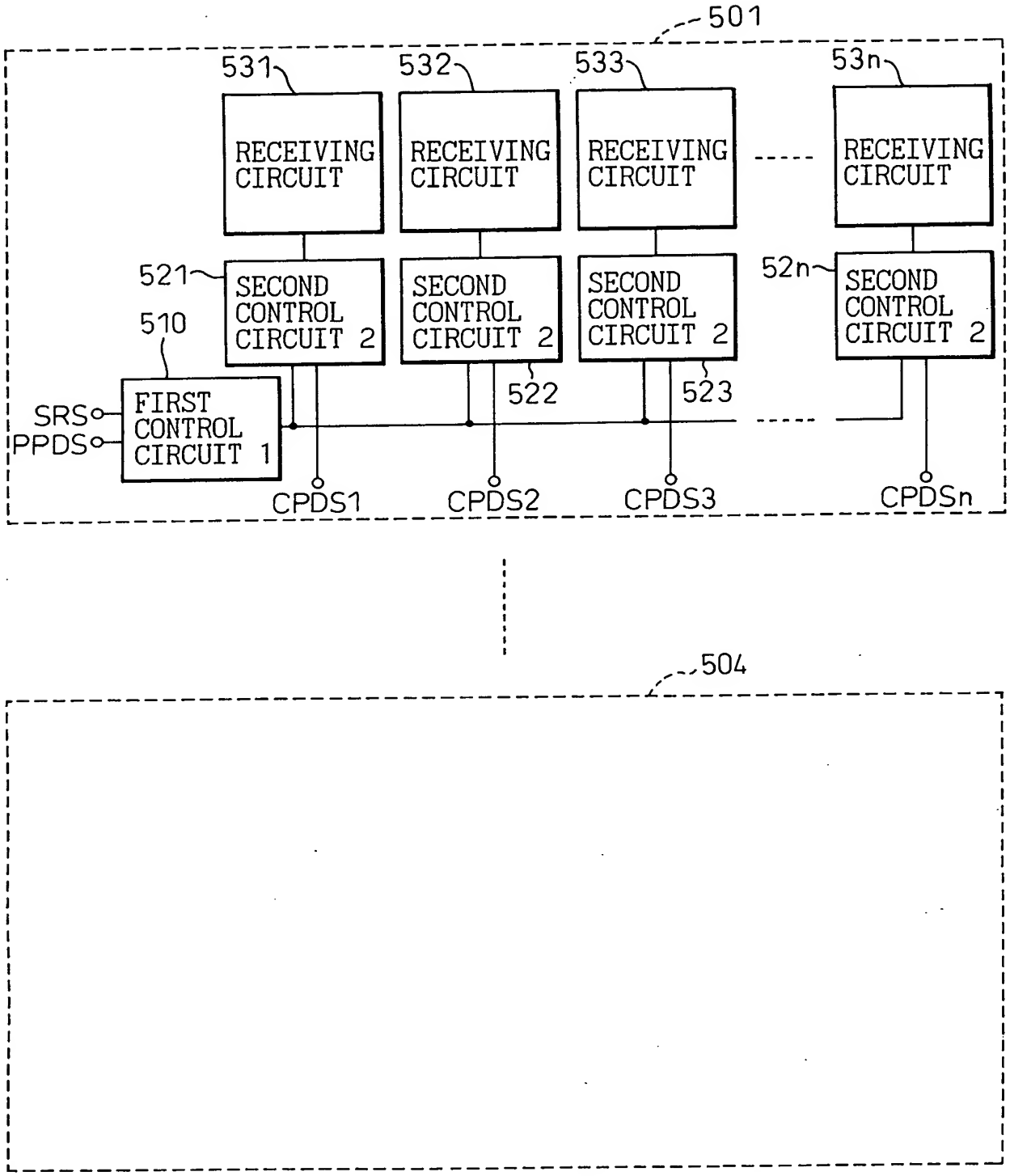
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533
53n
RECEIVING CIRCUIT
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SECOND CONTROL CIRCUIT 2
SECOND CONTROL CIRCUIT 2
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SRS
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FIRST CONTROL CIRCUIT 1
CPDS1
CPDS2
CPDS3
CPDSn
504

Fig.25A

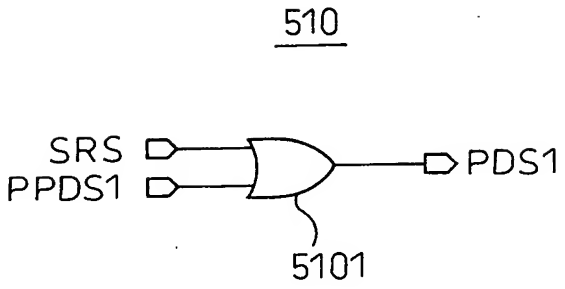
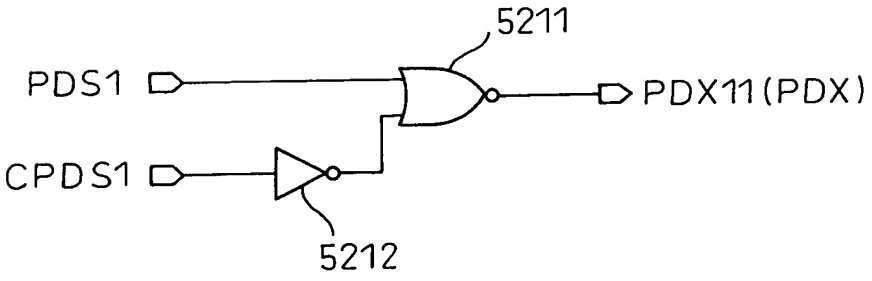
Fig.25B